That which is claimed is:

1. A method for forming an electronic structure comprising:

forming a seed layer on the electronic substrate;

forming a conductive shunt layer on portions of the seed layer wherein portions of the seed layer are free of the conductive shunt layer wherein the conductive shunt layer comprises a first material; and

forming a solder layer on the conductive shunt layer wherein the solder layer comprises a second material different than the first material.

2. A method according to Claim 1 further comprising:

after forming the solder layer, removing portions of the seed layer free of the solder layer.

3. A method according to Claim 1 wherein the conductive shunt layer comprises copper.

4. A method according to Claim 1 wherein the conductive shunt layer comprises a metal layer having a thickness of at least approximately 0.5μm.

5 A method according to Claim 4 further comprising:

heating the solder layer above its melting temperature while maintaining the conductive shunt layer having the thickness of at least approximately 0.5μm; and

after heating the solder layer, cooling the solder layer below its melting temperature while maintaining the conductive shunt layer having the thickness of at least approximately 0.5μm after cooling the solder layer below its melting temperature.

6. A method according to Claim 4 wherein the conductive shunt layer comprises a metal layer having a thickness of at least approximately 1.0μm.

7. A method according to Claim 6 wherein the conductive shunt layer comprises a metal layer having a thickness in the range of approximately 1.0μm to 5.0μ.

8. A method according to Claim 1 further comprising:

before forming the solder layer, forming a conductive barrier layer on the conductive shunt layer opposite the seed layer wherein the barrier layer comprises a third material different than the first and second materials.

9. A method according to Claim 8 wherein the barrier layer comprises at least one of nickel, platinum, palladium and/or combinations thereof.

10. A method according to Claim 1 wherein the seed layer comprises an adhesion layer of a third material different than the first material of the conductive shunt layer.

11. A method according to Claim 10 wherein the adhesion layer comprises titanium, tungsten, chrome, and/or combinations thereof.

12. A method according to Claim 10 wherein the seed layer comprises a plating conduction layer on the adhesion layer opposite the substrate, wherein the plating conduction layer comprises the first material of the conductive shunt layer.

13. A method according to Claim 1 further comprising:

after forming the seed layer, forming a mask layer on the seed layer, the mask layer having a pattern exposing a surface portion of the seed layer;

wherein forming the conductive shunt layer comprises plating the conductive shunt layer on the exposed surface portion of the seed layer; and

wherein forming the solder layer comprises plating the solder layer on the conductive shunt layer.

14. A method according to Claim 1 further comprising:

forming a conductive pad on a substrate; and

forming an insulating layer on the substrate and on the conductive pad, the insulating layer having a via therein so that a portion of the conductive pad opposite the substrate is free of the insulating layer;

wherein the seed layer is on the insulating layer, on sidewalls of the via, and on the portions of the conductive pad free of the insulating layer, and wherein the conductive shunt layer is on the seed layer opposite the portions of the conductive pad free of the insulating layer, opposite the sidewalls of the via, and opposite portions of the insulating layer adjacent the via.

15. A method according to Claim 14 further comprising:

forming a primary conductive trace on the substrate so that the primary conductive trace is between the substrate and the insulating layer; and

forming an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing at least two separate current flow paths between the primary conductive trace and the conductive pad.

16. A method of forming an electronic structure comprising:

forming a conductive pad on a substrate;

forming an insulating layer on the substrate and on the conductive pad, the insulating layer having a via therein so that a portion of the conductive pad opposite the substrate is free of the insulating layer;

forming a conductive shunt layer on the portion of the conductive pad free of the insulating layer, on sidewalls of the via, and on surface portions of the insulating layer surrounding the via opposite the substrate and the conductive pad, wherein the conductive shunt layer has a thickness of at least approximately 0.5μm; and

forming a solder layer on the barrier layer opposite the conductive shunt layer wherein solder layer and the conductive shunt layer comprise different materials.

17. A method according to Claim 16 further comprising:

heating the solder layer above its melting temperature while maintaining the conductive shunt layer having the thickness of at least approximately 0.5μm; and

cooling the solder layer below its melting temperature while maintaining the conductive shunt layer having the thickness of at least approximately 0.5μm after cooling the solder layer below its melting temperature.

18. A method according to Claim 16 wherein the conductive shunt layer has a thickness of at least approximately 1.0μm.

19. A method according to Claim 18 wherein the conductive shunt layer has a thickness in the range of approximately 1.0μm to 5.0μm.

20. A method according to Claim 16 further comprising:

before forming the conductive shunt layer, forming a seed layer on the conductive pad and on the insulating layer so that the seed layer is between the conductive shunt layer and the portion of the conductive pad free of the insulating layer and so that the seed layer is between the conductive shunt layer and the insulating layer.

21. A method according to Claim 20 wherein the seed layer comprises an adhesion layer of a material different than that of the conductive shunt layer.

22. A method according to Claim 21 wherein the adhesion layer comprises titanium, tungsten, chrome, and/or combinations thereof.

23. A method according to Claim 21 wherein the seed layer comprises a plating conduction layer on the adhesion layer opposite the substrate, wherein the plating conduction layer and the conductive shunt layer comprise a common material.

24. A method according to Claim 20 wherein the conductive shunt layer, and the solder layer are on portions of the seed layer, and wherein portions of the seed layer are free of the conductive shunt layer, and the solder layer.

25. A method according to Claim 24 further comprising:

after forming the solder layer, removing portions of the seed layer free of the conductive shunt layer and the solder layer.

26. A method according to Claim 20 further comprising:

after forming the seed layer, forming a mask layer on the seed layer, the mask layer having a pattern exposing a surface portion of the seed layer opposite the portion of the conductive pad free of the insulating layer, opposite sidewalls of the via, and opposite surface portions of the insulating layer surrounding the via;

wherein forming the conductive shunt layer comprises plating the conductive shunt layer on the exposed portion of the seed layer; and

wherein forming the solder layer comprises plating the solder layer on the conductive shunt layer.

27. A method according to Claim 26 further comprising:

after forming the solder layer, removing the mask layer; and

after removing the mask layer, removing portions of the seed layer surrounding the conductive shunt layer.

28. A method according to Claim 16 wherein the conductive shunt layer comprises copper.

29. A method according to Claim 16 further comprising:

forming a conductive barrier layer on the conductive shunt layer opposite the conductive pad and the insulating layer wherein the conductive shunt layer and the barrier layer comprise different materials.

30. A method according to Claim 29 wherein the conductive barrier layer comprises nickel, palladium, platinum, and/or combinations thereof.

31. A method according to Claim 16 further comprising:

forming a primary conductive trace on the substrate so that the primary conductive trace is between the substrate and the insulating layer; and

forming an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing at least two separate current flow paths between the primary conductive trace and the conductive pad.

32. An electronic structure comprising:

an electronic substrate;

a seed layer on the electronic substrate;

a conductive shunt layer on portions of the seed layer wherein portions of the seed layer are free of the conductive shunt layer wherein the conductive shunt layer comprises a first material; and

a solder layer on the conductive shunt layer wherein the solder layer comprises a second material different than the first material.

33. An electronic structure according to Claim 32 further comprising:

a conductive pad on the substrate; and

an insulating layer on the substrate and on the conductive pad, the insulating layer having a via therein so that a portion of the conductive pad opposite the substrate is free of the insulating layer;

wherein the seed layer is on the insulating layer, on sidewalls of the via, and on the portions of the conductive pad free of the insulating layer, and wherein the conductive shunt layer is on the seed layer opposite the portions of the conductive pad free of the insulating layer, opposite the sidewalls of the via, and opposite portions of the insulating layer adjacent the via.

34. A method according to Claim 33 further comprising:

a primary conductive trace on the substrate so that the primary conductive trace is between the substrate and the insulating layer; and

an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing at least two separate current flow paths between the primary conductive trace and the conductive pad.

35. An electronic structure according to Claim 32 wherein the conductive shunt layer comprises copper.

36. An electronic structure according to Claim 32 wherein the conductive shunt layer comprises a metal layer having a thickness of at least approximately 0.5μm.

37. An electronic structure according to Claim 36 wherein the solder layer has a rounded surface opposite the conductive shunt layer having the thickness of at least approximately 0.5μm.

38. An electronic structure according to Claim 36 wherein the conductive shunt layer comprises a metal layer having a thickness of at least approximately 1.0μm.

39. An electronic structure according to Claim 38 wherein the conductive shunt layer comprises a metal layer having a thickness in the range of approximately 1.0μm to 5.0μm.

40. An electronic structure according to Claim 32 further comprising:

a conductive barrier layer between the conductive shunt layer and the solder layer wherein the conductive barrier layer comprises a third material different than the first and second materials.

41. An electronic structure according to Claim 40 wherein the barrier layer comprises at least one of nickel, platinum, palladium, and/or combinations thereof.

42. An electronic structure according to Claim 32 wherein the seed layer comprises an adhesion layer of a third material different than the first material of the conductive shunt layer.

43. An electronic structure according to Claim 42 wherein the adhesion layer comprises titanium, tungsten, chrome, and/or combinations thereof.

44. An electronic structure according to Claim 42 wherein the seed layer comprises a plating conduction layer on the adhesion layer opposite the substrate, wherein the plating conduction layer comprises the first material of the conductive shunt layer.

45. An electronic structure comprising:

a conductive pad on a substrate;

a insulating layer on the substrate and on the conductive pad, the insulating layer having a via therein so that a portion of the conductive pad opposite the substrate is free of the insulating layer;

a conductive shunt layer on the portion of the conductive pad free of the insulating layer, on sidewalls of the via, and on surface portions of the insulating layer surrounding the via opposite the substrate and the conductive pad, wherein the conductive shunt layer has a thickness of at least approximately 0.5μm; and

a solder layer on the conductive shunt layer wherein the conductive shunt layer and the solder layer comprise different materials.

46. An electronic structure according to Claim 45 wherein the solder layer has a rounded surface opposite the conductive shunt layer having the thickness of at least approximately 0.5μm.

47. An electronic structure according to Claim 45 wherein the conductive shunt layer has a thickness of at least approximately 1.0μm.

48. An electronic structure according to Claim 45 wherein the conductive shunt layer has a thickness in the range of approximately 1.0μm to 5.0μm.

49. An electronic structure according to Claim 45 wherein the conductive shunt layer comprises copper.

50. An electronic structure according to Claim 45 further comprising:

a seed between the conductive shunt layer and the conductive pad and between the conductive shunt layer and the insulating layer.

51. An electronic structure according to Claim 50 wherein the seed layer comprises an adhesion layer of a material different than that of the conductive shunt layer.

52. An electronic structure according to Claim 51 wherein the adhesion layer comprises titanium, tungsten, chrome, and/or combinations thereof.

53. An electronic structure according to Claim 51 wherein the seed layer comprises a plating conduction layer on the adhesion layer opposite the substrate, wherein the plating conduction layer and the conductive shunt layer comprise a common material.

54. An electronic structure according to Claim 50 wherein the conductive shunt layer, the conductive barrier layer, and the solder layer are on portions of the seed layer, and wherein portions of the seed layer are free of the conductive shunt layer, the conductive barrier layer, and the solder layer.

55. An electronic structure according to Claim 45 further comprising:

a conductive barrier layer between the conductive shunt layer and the solder layer wherein the conductive shunt layer and the barrier layer comprise different materials.

56. An electronic structure according to Claim 55 wherein the conductive barrier layer comprises at least one of nickel, platinum, palladium, and/or combinations thereof.

57. An electronic structure according to Claim 45 further comprising:

a primary conductive trace on the substrate so that the primary conductive trace is between the substrate and the insulating layer; and

an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing at least two separate current flow paths between the primary conductive trace and the conductive pad.

58. An electronic structure comprising:

an electronic substrate;

a primary conductive trace on the electronic substrate, the primary conductive trace having a first width;

a conductive pad on the electronic substrate, the conductive pad having a second width greater than the first width; and

an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing at least two separate current flow paths between the primary conductive trace and the conductive pad.

59. An electronic structure according to Claim 58 wherein the electrical coupling comprises a flared coupling extending from the primary conductive trace to the conductive pad and having a perforation therein.

60. An electronic structure according to Claim 58 wherein the electrical coupling comprises first and second traces extending from the primary conductive trace to spaced apart portions of the conductive pad.

61. An electronic structure according to Claim 60 wherein the first and second traces extend to opposite sides of the conductive pad.

62. An electronic structure according to Claim 60 wherein the conductive pad is circular and wherein the first and second traces extend tangentially from different portions of the circular conductive pad and meet at the primary conductive trace.

63. An electronic structure according to Claim 60 wherein the first and second traces extend from the circular pad in parallel directions and turn to meet at the primary conductive trace.

64. An electronic structure according to Claim 60 wherein the electrical coupling further comprises a third trace extending from the primary conductive trace to the conductive pad between the first and second traces.

65. An electronic structure according to Claim 64 wherein the third trace has a width that is less than a width of either of the first and second traces.

66. An electronic structure according to Claim 60 further comprising:

a solder layer on the conductive pad; and

a second electronic substrate on the solder layer wherein at least one of the first and second traces is coupled to the conductive pad adjacent to a portion of the solder layer subject to compressive stress.

67. An electronic structure according to Claim 58 further comprising:
an insulating layer on the electronic substrate, on the conductive trace, on the conductive pad, and on the electrical coupling, the insulating layer having a via therein so that a portion of the conductive pad is free of the insulating layer.

68. An electronic structure according to Claim 58 wherein the electronic substrate includes a semiconductor substrate, a contact pad on the semiconductor substrate, and an insulating layer on the semiconductor substrate and the contact pad, the insulating layer having a via therein so that a portion of the contact pad is free of the insulating layer, wherein the conductive trace, the conductive pad, and the electrical coupling are on the insulating layer opposite the substrate, and wherein the conductive trace is electrically coupled with the contact pad through the via.

69. An electronic structure according to Claim 58 further comprising;
an insulating layer on the electronic substrate, the primary conductive trace, the conductive pad, and the electrical coupling, the insulating layer including a via therein so that portions of the conductive pad are free of the insulating layer;
a conductive shunt layer on the portions of the conductive pad free of the insulating layer, on sidewalls of the via, and on portions of the insulating layer adjacent the via; and
a solder layer on the conductive shunt layer opposite the substrate.

70. A method of forming an electronic structure, the method comprising:
forming a primary conductive trace on an electronic substrate, the primary conductive trace having a first width;
forming a conductive pad on the electronic substrate, the conductive pad having a second width greater than the first width; and
forming an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing at least two separate current flow paths between the primary conductive trace and the conductive pad.

71. A method according to Claim 70 wherein the electrical coupling comprises a flared coupling extending from the primary conductive trace to the conductive pad and having a perforation therein.

72. A method according to Claim 70 wherein the electrical coupling comprises first and second traces extending from the primary conductive trace to spaced apart portions of the conductive pad.

73. A method according to Claim 72 wherein the first and second traces extend to opposite sides of the conductive pad.

74. A method according to Claim 72 wherein the conductive pad is circular and wherein the first and second traces extend tangentially from different portions of the circular conductive pad and meet at the primary conductive trace.

75. A method according to Claim 72 wherein the first and second traces extend from the circular pad in parallel directions and turn to meet at the primary conductive trace.

76. A method according to Claim 72 wherein the electrical coupling further comprises a third trace extending from the primary conductive trace to the conductive pad between the first and second traces.

77. A method according to Claim 76 wherein the third trace has a width that is less than a width of either of the first and second traces.

78. A method according to Claim 72 further comprising:

forming a solder layer on the conductive pad; and

providing a second electronic substrate on the solder layer wherein at least one of the first and second traces is coupled to the conductive pad adjacent to a portion of the solder layer subject to compressive stress.

79. A method according to Claim 70 further comprising:

forming an insulating layer on the electronic substrate, on the conductive trace, on the conductive pad, and on the electrical coupling, the insulating layer having a via therein so that a portion of the conductive pad is free of the insulating layer.

80. A method according to Claim 70 wherein the electronic substrate includes a semiconductor substrate, a contact pad on the semiconductor substrate, and an insulating layer on the semiconductor substrate and the contact pad, the insulating layer having a via therein so that a portion of the contact pad is free of the insulating layer, wherein the conductive trace, the conductive pad, and the electrical coupling are on the insulating layer opposite the substrate, and wherein the conductive trace is electrically coupled with the contact pad through the via.

81. A method according to Claim 70 further comprising;

forming an insulating layer on the electronic substrate, the primary conductive trace, the conductive pad, and the electrical coupling, the insulating layer including a via therein so that portions of the conductive pad are free of the insulating layer;

forming a conductive shunt layer on the portions of the conductive pad free of the insulating layer, on sidewalls of the via, and on portions of the insulating layer adjacent the via; and

forming a solder layer on the conductive shunt layer opposite the substrate.

82. An electronic structure comprising:

an electronic substrate;

a primary conductive trace on the electronic substrate, the primary conductive trace having a first width;

a conductive pad on the electronic substrate, the conductive pad having a second width greater than the first width; and

an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing different resistances to current flow across a width thereof.

83. An electronic structure according to Claim 82 wherein the electrical coupling has an opening therein.

84. An electronic structure according to Claim 82 wherein the electrical coupling has different thicknesses across a width thereof.

85. An electronic structure according to Claim 82 wherein the electrical coupling includes a layer of a first conductive material in a central portion thereof and a layer of a second conductive material along peripheral portions thereof the first and second conductive materials having different resistivities.

86. An electronic structure according to Claim 85 wherein the layer of the second conductive material extends across the electrical coupling on the layer of the first conductive material.

87. An electronic structure according to Claim 82 wherein the electrical coupling provides uniform distribution of current for the conductive pad.

88. A method of forming an electronic structure, the method comprising:

forming an electronic substrate;

forming a primary conductive trace on the electronic substrate, the primary conductive trace having a first width;

forming a conductive pad on the electronic substrate, the conductive pad having a second width greater than the first width; and

forming an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing different resistances to current flow across a width thereof.

89. A method according to Claim 88 wherein the electrical coupling has an opening therein.

90. A method according to Claim 88 wherein the electrical coupling has different thicknesses across a width thereof.

91. A method according to Claim 88 wherein the electrical coupling includes a layer of a first conductive material in a central portion thereof and a layer of a

second conductive material along peripheral portions thereof the first and second conductive materials having different resistivities.

92. A method according to Claim 85 wherein the layer of the second conductive material extends across the electrical coupling on the layer of the first conductive material.

93. A method according to Claim 88 wherein the electrical coupling provides uniform distribution of current for the conductive pad.